MEINBERG

Technical Information

Operating Instructions

VME31

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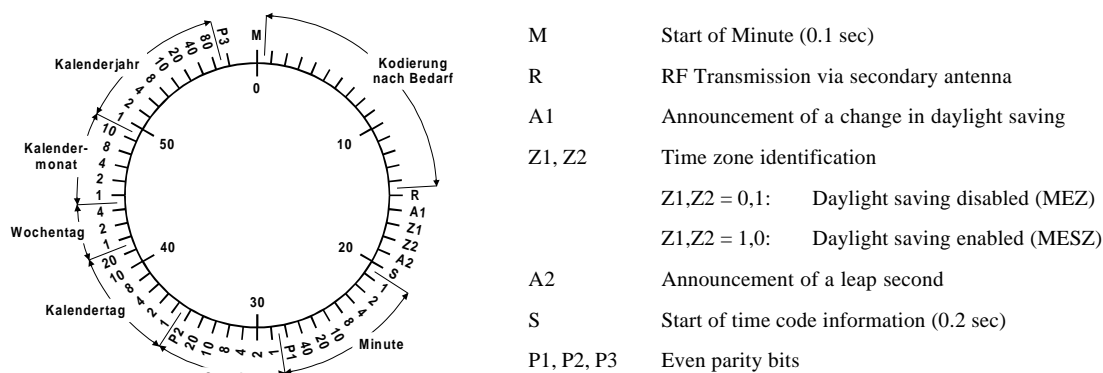# Table of Contents

General Information about DCF77

The radio remote clocks made by Meinberg receive the signal from the long wave transmitter DCF77. This long wave transmitter installed in Mainflingen near Frankfurt/Germany transmits the reference time of the Federal Republic of Germany. This time reference is either the Central European Time (Mitteleuropäische Zeit, MEZ) or the Central European Summer Time (Mitteleuropäische Sommerzeit, MESZ). The transmitter is controlled by the atomic clock plant at the Federal Physical Technical Institute (PTB) in Braunschweig/Germany and transmits the current time of day, date of month and day of week in coded second pulses. Once every minute the complete time information is available.

At the beginning of every second the amplitude of the high precision 77.5 kHz carrier frequency is lowered by 75% for a period of 0.1 or 0.2 sec. The length of these time marks represent a binary coding scheme using the short time mark for logical zeroes and the long time mark for logical ones. The information on the current date and time as well as some parity and status bits can be decoded from the time marks of the 15th up to the 58th second every minute. The absence of any time mark at the 59th second of a minute signals that a new minute will begin with the next time mark.

Our radio remote clocks decode the highly accurate information on date and time within a wide range around Germany. So some of our clocks are installed in Bilbao/Spain as well as in the city of Umeå in northern Sweden - fully satisfying the requirements of the users. The radio remote clocks automatically switch to summertime and back. The reception of the time information is free of charge and does not need to be registered.

Generally it is important to position the antenna in an optimal way. It should be mounted at least 30 centimeters away from the clock unit and from solid steel. The antenna should be aligned at a right angle to the direction of the transmitter (Frankfurt).

Figure: Decoding Scheme

|	
M	Start of Minute (0.1 sec)
R	RF Transmission via secondary antenna
A1	Announcement of a change in daylight saving
Z1, Z2	Time zone identification
	Z1,Z2 = 0,1: Daylight saving disabled (MEZ)
	Z1,Z2 = 1,0: Daylight saving enabled (MESZ)
A2	Announcement of a leap second
S	Start of time code information (0.2 sec)
P1, P2, P3	Even parity bits

Overview

The radio remote clock DCF77 VME31 receives the time marks from DCF77 and makes the decoded time available to VME bus systems. The clock is designed on a 3U board (euro card size), so it can be used in either 3U systems or 6U systems. An external ferrit antenna passes the signal from DCF77 to the on-board long wave receiver. The demodulated time marks are decoded by the clock´s microprocessor. If no errors are detected in the current time message, an additional plausibility check against the previous time message is performed. If that plausibility check passes, too, the battery buffered real time clock on the board is synchronized corresponding to the decoded time and date.

Software running on the computer can read out the date/time/status and some more information from the board's dual port RAM which is updated in 10ms intervals. The dual port RAM can be configured by a block of jumpers to be mapped to any 1k boundary in the system's A16 address range. It can be accessed using either Short Supervisor I/O (2Dh) or Short Non-Priviledged I/O (29H). The radio remote clock can generate cyclic interrupts at one of the levels IRQ1 through IRQ7 at a rate of 10ms, 100 ms, 1s, 10s, 60s, or 1h.

Frontansicht

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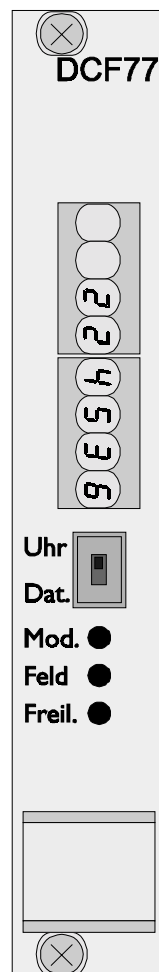
Configuration

Before the board can be installed in the VME bus rack, some jumpers must be configured as described below. The location of the jumpers can be seen from the component layout at the end of this manual.

Setting the Base Address

The base address of the dual port RAM on the board must be configured corresponding to the table shown below:

Adressdecodierung VME31

J15	J14	J13	J12	J11	J10	
*	*	*	*	*	*	0000H
*	*	*	*	*	–	0400H
*	*	*	*	–	*	0800H
*	*	*	*	–	–	0C00H
*	*	*	–	*	*	1000H
*	*	*	–	*	–	1400H
*	*	*	–	–	*	1800H
*	*	*	–	–	–	1C00H
*	*	–	*	*	*	2000H
*	*	–	*	*	–	2400H
*	*	–	*	–	*	2800H
*	*	–	*	–	–	2C00H
*	*	–	–	*	*	3000H
*	*	–	–	*	–	3400H
*	*	–	–	–	*	3800H
*	*	–	–	–	–	3C00H
*	–	*	*	*	*	4000H
*	–	*	*	*	–	4400H
*	–	*	*	–	*	4800H
*	–	*	*	–	–	4C00H
*	–	*	–	*	*	5000H
*	–	*	–	*	–	5400H
*	–	*	–	–	*	5800H
*	–	*	–	–	–	5C00H
*	–	–	*	*	*	6000H
*	–	–	*	*	–	6400H
*	–	–	*	–	*	6800H
*	–	–	*	–	–	6C00H
*	–	–	–	*	*	7000H
*	–	–	–	*	–	7400H
*	–	–	–	–	*	7800H
*	–	–	–	–	–	7C00H
–	*	*	*	*	*	8000H
–	*	*	*	*	–	8400H
–	*	*	*	–	*	8800H
–	*	*	*	–	–	8C00H
–	*	*	–	*	*	9000H
–	*	*	–	*	–	9400H
–	*	*	–	–	*	9800H
–	*	*	–	–	–	9C00H
–	*	–	*	*	*	A000H
–	*	–	*	*	–	A400H
–	*	–	*	–	*	A800H
–	*	–	*	–	–	AC00H
–	*	–	–	*	*	B000H
–	*	–	–	*	–	B400H
–	*	–	–	–	*	B800H
–	*	–	–	–	–	BC00H
–	–	*	*	*	*	C000H
–	–	*	*	*	–	C400H
–	–	*	*	–	*	C800H
–	–	*	*	–	–	CC00H
–	–	*	–	*	*	D000H
–	–	*	–	*	–	D400H
–	–	*	–	–	*	D800H
–	–	*	–	–	–	DC00H
–	–	–	*	*	*	E000H
–	–	–	*	*	–	E400H
–	–	–	*	–	*	E800H
–	–	–	*	–	–	EC00H
–	–	–	–	*	*	F000H
–	–	–	–	*	–	F400H
–	–	–	–	–	*	F800H
–	–	–	–	–	–	FC00H

*: Jumper gesetzt

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Selecting the I/O Access Mode

An additional jumper J1 must be configured to select the access mode: if the jumper is installed, the board can be accessed using Short Supervisor I/O (2Dh), otherwise the board is accessed using Short Non-Priviledged I/O (29h).

Installation

After the jumpers have been configured, the board can be installed in the VME bus rack. When the system is turned on, the clock starts displaying either the on-board date or time, depending on the position of the date/time selection switch. The LEDs let the user check the clock's status and proper receiver operation.

It is important to position the antenna in an optimal way. The antenna should be installed at least 30 centimeters away from the clock board and from solid steel. It should be aligned at a right angle to the direction of the transmitter (Frankfurt).

If the antenna is connected, the brightness of the green LED labeled **Feld** reflects the strength of the RF signal. A good way to align the antenna is to turn it **slowly** until this LED is mostly dimmed due to minimum signal, finally, the antenna is turned by a 90° angle to obtain maximum signal.

If the antenna is properly installed, the green LED labeled **Mod.** should be blinking exactly once per second corresponding to the time marks from DCF77. If this LED flashes, there is some electrical noise around which prevents the receiver from decoding the time marks and synchronizing.

The red LED labeled **Freil.** is on if the clock is running on xtal. This LED can only change when the minute changes (seconds increment from 59 to 0). After power-up, it takes at least two up to three minutes until this LED is turned off.

Interface Description

Information on date, time, and status is made available to the VME bus via dual port RAM. The dual port RAM is mapped into the VME bus' A16 address range corresponding to the jumper settings described above. The contents of the dual port RAM is updated once every 10ms.

Care must be taken not to read an inconsistent block of data due to an update cycle occurring in the middle of the read loop. For example, the 100th-of-seconds value could be read twice: as the first byte, and, again, as the last byte. If both of the values are identical, no update has taken place while the read loop was executed. Another

method is to read the clock interrupt driven or poll the 100th-of-seconds until the value changes: in both of the cases, the software has an interval of 10ms to read the desired data.

Address Map

The VME31 radio remote clock has a A16:D8 bus interface, so the dual port RAM must be accessed byte wide on odd address offsets related to the base address. The address map is shown below:

01h	(reserved)
03h	(reserved)
05h	interrupt vector (default: 0Fh)
07h	interrupt level (00h..07h, default: 00h - disabled)
09h	interrupt rate (default: 00h, see below)
0Bh	EPROM ID
0Dh	status (see below)
0Fh	year (00h..99h)
11h	month (01h..12h)
13h	day-of-month (01h..31h)
15h	hour (00h..23h)
17h	minute (00h..59h)
19h	second (00h..59h)
1Bh	sec100 (00h..99h)
1Dh	day-of-week (01h..07h, 01h = Monday)
1Fh	(reserved)

Date and time values are represented in packed BCD numbers.

The bits of the status byte are defined as described below:

bit	stands for	"1"	"0"
D0	clock´s current state:	free running	DCF77 controlled
D1	daylight saving:	enabled	disabled
D2	Sync´ed since last Reset:	yes	no
D3	dayl. saving going to change:	yes	no
D4	interrupt	enabled	disabled
D5	(reserved, always "0")		
D6	(reserved, always "0")		
D7	on-board RTC time invalid:	yes	no

Using Periodic Interrupts

If the clock shall generate periodic interrupts, three bytes must be written to the dual port RAM:

Interrupt Vector

After power up, this byte is set to 0Fh. The user must take care to set up the vector number corresponding to the system's exception vector assignments.

Interrupt Level

This byte is set to 00h after power up. The user must supply the desired interrupt level (01h..07h).

Interrupt Rate

The contents of this byte reflects the rate of interrupts generated by the board. After power up, its value is 00h. Valid codes are given below:

00h	no interrupt
01h	once ever 10 milliseconds
02h	once every 100 milliseconds
03h	once every second
04h	on every 10 seconds
05h	once every minute
06h	once every 10 minutes
07h	once every hours
others:	(reserved)

Technical Specifications

RECEIVER:	Narrow bandwidth receiver with automatic gain control Bandwidth: approx. 40Hz

ANTENNA:	Active external ferrite antenna in a plastic case
	  Length of the cable: up to more than 100m
	
	Standard:
	  SMB type connector, 5m of RG174 cable
	
	Outdoor:
	  N type connector, RG58 cable, adapter RG58/RG174

DISPLAY:	eight digit LED display shows date or time (selectable by switch)
RF AMPLITUDE, MODULATION:	Indicated by LEDs
TIMECODE CHECK:	Parity and consistency checking over a period of two minutes RF distortions indicated by both LED and a bit of the status register Without RF signal the clock runs on XTAL with an accuracy of 10^{-5}
BATTERY BACKUP:	NiCd accu when the computer is turned off, the on-board RTC keeps the time based on XTAL for more than four weeks
RELIABILITY OF OPERATION:	Microprocessor supervisory circuit provides watchdog timer, power supply monitoring and backup-battery switchover

SYSTEM BUS
INTERFACE: VME bus A16:D8, slave
                Access: Short Supervisor I/O (2Dh)
                                      Short Non-priviledged I/O (29h)
                IRQ levels: 1..7, programmable

DATA FORMAT: packed BCD

PERIODIC
INTERRUPTS: none, 10ms, 100ms, 1s, 10s, 1min, 10min, or 1h

POWER
REQUIREMENT: +5V @ 320mA

PHYSICAL
DIMENSION: 3U Euro card, 6U front panel optional
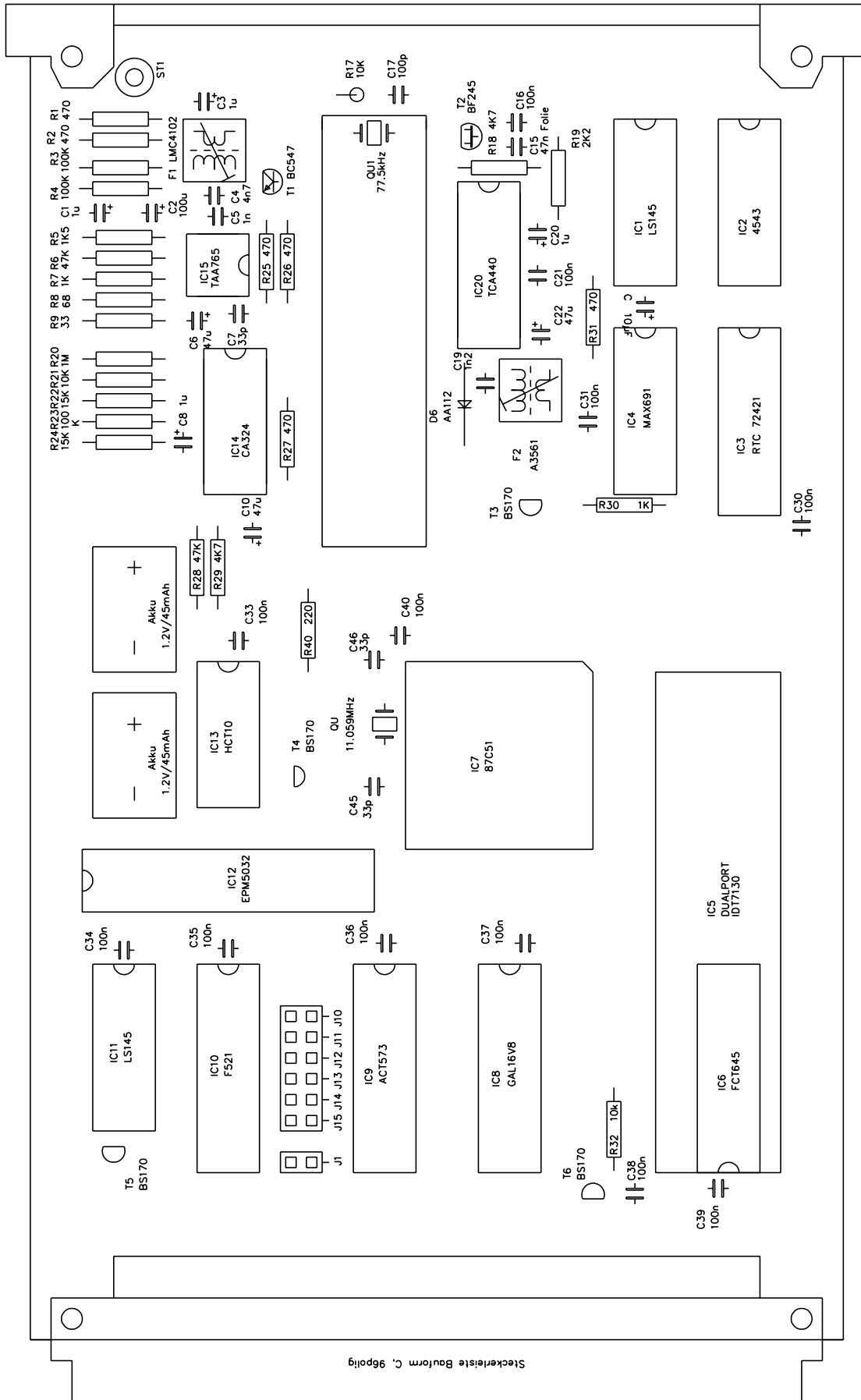
AMBIENT
TEMPERATURE: 0 ... 50°C

HUMIDITY: max. 85 %

CE Label

This device conforms to the directive 89/336/EWG on the approximation of the laws of the Member States of the European Community relating to electromagnetc compatibility.

Component Layout

MEINBERG Best.Plan VME 31

Pin Assignments

	a	b	c
1	D0		
2	D1		
3	D2		
4	D3	/BG0IN	
5	D4	/BG0OUT	
6	D5	/BG1IN	
7	D6	/BG1OUT	
8	D7	/BG2IN	
9	GND	/BG2OUT	GND
10	SYSCLK	/BG3IN	/SYSFAIL
11	GND	/BG3OUT	/BERR
12			/SYSRESET
13	/DS0		/LWORD
14	/WRITE		AM5
15	GND		
16	/DTACK	AM0	
17	GND	AM1	
18	/AS	AM2	
19	GND	AM3	
20	/IACK	GND	
21	/IACKIN		
22	/IACKOUT		
23	AM4	GND	A15
24		/IRQ7	A14
25		/IRQ6	A13
26		/IRQ5	A12
27	A4	/IRQ4	A11
28	A3	/IRQ3	A10
29	A2	/IRQ2	
30	A1	/IRQ1	
31			
32	VCC in (+5V)	VCC in (+5V)	VCC in (+5V)